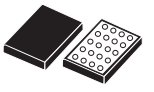
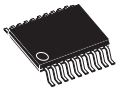
ST2378E

8-BIT DUAL SUPPLY 1.71V TO 5.5V LEVEL TRANSLATOR WITH I/OV_{CC} ±15KV ESD PROTECTION

- HIGH SPEED: t_{PD} = 15ns (MAX.) at T_A = 85°C
  V_L = 1.8V; V_{CC} = 5.5V
- GUARANTEED DATA RATE:
  13Mbps (1.8V ≤ V_L ≤ V_{CC} ≤ 5.5V)
- LOW POWER DISSIPATION:
  I_{TS-VL} = I_{TS-VCC} = 1µA (MAX.) at T_A = 85°C
  I_{QVL} = 100µA (MAX.) at T_A = 85°C
  I_{QCC} = 10µA (MAX.) at T_A = 85°C
- OUTPUT IMPEDANCE:
  $|I_{OHA}|$ = 20 µA (MIN.) at V_L=1.8V V_{CC}=5.5V
  I_{OLA} = 1.0 mA (MIN.) at V_L=1.8V V_{CC}=5.5V
- BIDIRECTIONAL LEVEL TRANSLATION
- TOTEM POLE AND OPEN DRAIN DRIVING FOR I^2C COMMUNICATIONS
- 5V TOLERANT ON ENABLE PIN
- THERMAL SHORT-CIRCUIT PROTECTION
- WIDE OPERATING VOLTAGE RANGE:
  V_L(OPR) = 1.71V to V_{CC}
  V_{CC}(OPR) = 1.71V to 5.5V
- ESD PERFORMANCE:
  HBM > 15KV ESD PROTECTION ON I/O_{VCC} LINES
- LEADFREE FLIPCHIP AND TSSOP PACKAGES



Flip-Chip



TSSOP

DESCRIPTION

The ST2378E is a ±15kV ESD-protected level translator providing the level shifting necessary to allow data transfer in a multi-voltage system.

Externally applied voltages, V_{CC} and V_L, set the logic levels on either side of the device. It utilizes a transmission-gate-based design to allow data translation in either direction (V_L <-> V_{CC}) on any single data line. The ST2378E accepts V_L from +1.71V to V_{CC} and V_{CC} from +1.71V to +5.5V, making them ideal for data transfer between low-voltage ASICs/PLDs and higher voltage systems. The ST2378E has a three-state output mode that reduces supply current to less than 1µA, thermal short-circuit protection, and ±15kV ESD protection on the V_{CC} side for greater protection in applications that route signals externally.

The ST2378E operates at a guaranteed data rate of 13Mbps over the entire specified operating voltage range. Within specific voltage domains, higher data rates are possible.

Figure 1: Block Diagram

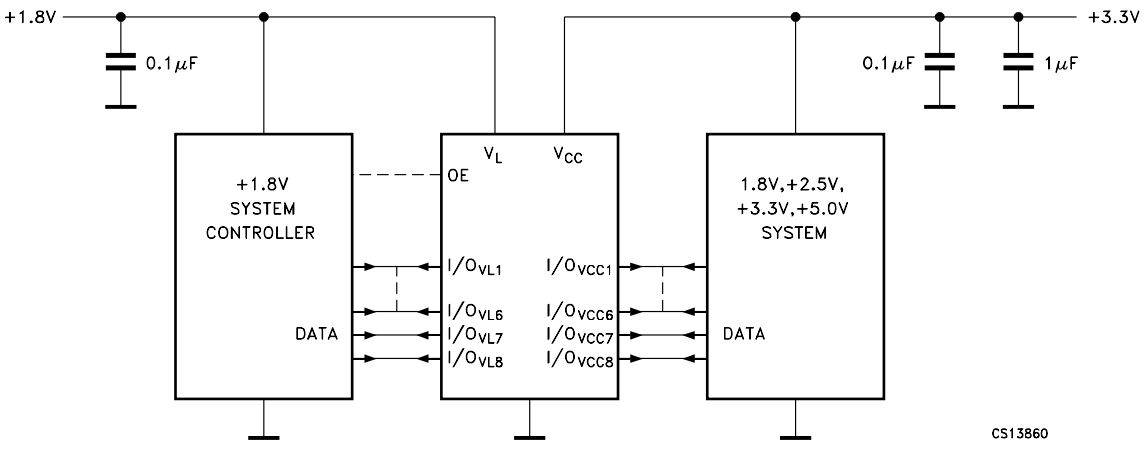


Figure 2: Functional Diagram (1 I/O LINE)

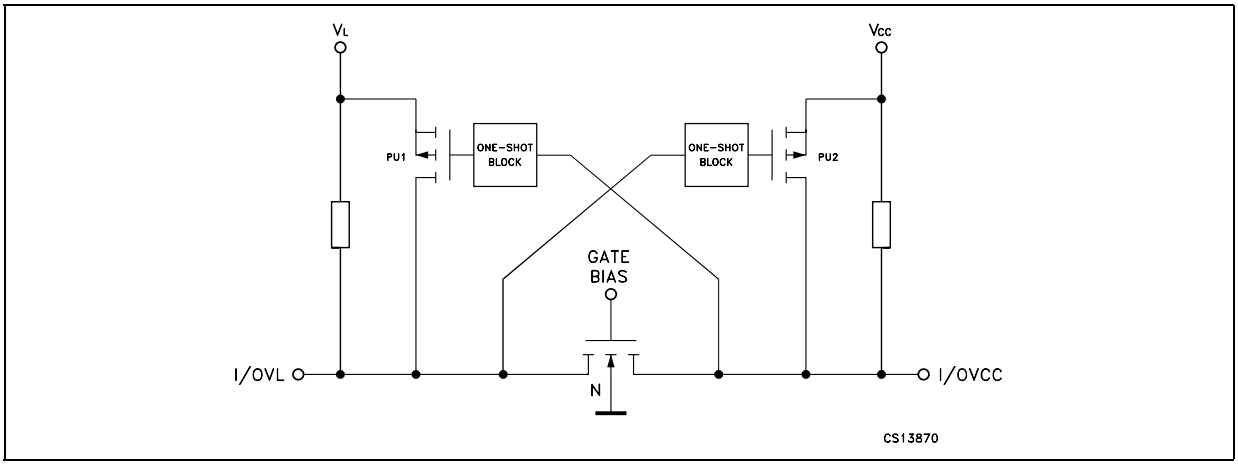


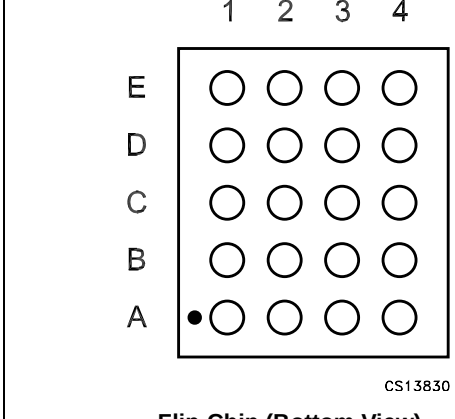
Table 1: Order Codes

Type	Temperature Range	Package	Comments
ST2378EBJR	-40 to 85 °C	Flip-Chip20 (Tape & Reel)	3000 parts per reel
ST2378ETTR	-40 to 85 °C	TSSOP20 (Tape & Reel)	2500 parts per reel

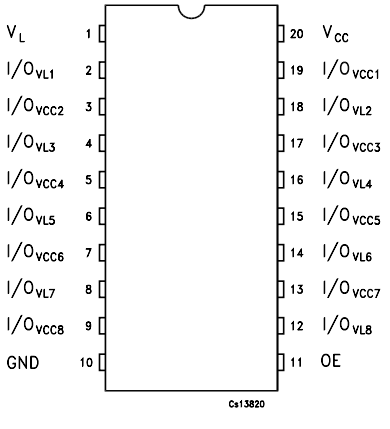
Table 2: Pin Description

FLIPCHIP20 PIN N°	TSSOP20 PIN N°	SYMBOL	NAME AND FUNCTION
E2, D1, D2, C1, C2, B1, B2, A1	2, 18, 4, 16, 6, 14, 8, 12	I/O_{VL1} to I/O_{VL8}	Data Inputs/Outputs
E3, D4, D3, C4, C3, B4, B3, A4	19, 3, 17, 5, 15, 7, 13, 9	I/O_{VCC1} to I/O_{VCC8}	Data Inputs/Outputs
A2	11	OE	Output Enable Inputs
A3	10	GND	Ground (0V)
E1	1	V_L	Positive Supply Voltage
E4	20	V_{CC}	Positive Supply Voltage

PIN CONFIGURATION



Flip-Chip (Bottom View)
Bump Side



TSSOP (Top View)

Table 3: Truth Table

Control Pin	Bidirectional Input/Outputs		Thermal Protection
OE	I/O_{VL}	I/O_{VCC}	
H(1)	H(1)	H(2)	Enabled
H(1)	L	L	Enabled
L	Z	Z	Disabled(3)

X=Don't care; Z=High Impedance;
1) High Level V_L Power Supply referred
2) High Level V_{CC} Power Supply referred
3) Thermal Protection disabled reduces the quiescent current consumption I_{TS-VCC}=I_{TS-VL}= 1µA Max at 85°C

Table 4: Absolute Maximum RatingS

Symbol	Parameter	Value	Unit
V_L	Supply Voltage	-0.3 to V_{CC}	V
V_{CC}	Supply Voltage	-0.3 to +7.0	V
V_{OE}	DC Control Input Voltage	-0.3 to +7.0	V
$V_{I/OVL}$	DC I/O_{VL} Input Voltage (OE = Gnd or V_L)	-0.3 to V_L + 0.3	V
$V_{I/OVCC}$	DC I/O_{VCC} Input Voltage (OE = Gnd or V_L)	-0.3 to V_{CC} + 0.3	V
I_{IK}	DC Input Diode Current (OE Control Pin)	– 20	mA
I_{IOVL}	DC Output Current	± 25	mA
I_{IOVCC}	DC Output Current	± 25	mA
I_{SCTOUT}	Short Circuit Duration I/O_{VL}, I/O_{VCC} Driven from 40mA Source	Continuous	mA
I_{CCB}	DC V_{CC} or Ground Current	± 100	mA
P_d	Power Dissipation(*)	500	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied
(*) 500mW: ≅ 65°C derated to 300mW by 10mW/°C: 65°C to 85°C

Table 5: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_L	Supply Voltage		1.71 to V_{CC}	V
V_{CC}	Supply Voltage		1.71 to 5.5	V
V_I	Input Voltage (OE Output Enable Pin, V_L Power Supply referred)		0 to 5.5	V
$V_{I/OVL}$	I/O_{VL} Voltage		0 to V_L	V
$V_{I/OVCC}$	I/O_{VCC} Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-40 to 85	°C
dt/dv	Input Rise and Fall Time (OE Control Pin) (1)		0 to 10	ns/V
dt/dv	Input Rise and Fall Time (2)	$1.71 < V_L < V_{CC} < 5V$	0 to 10	ns/V
		$V_{CC} = V_L = 5V$	0 to 3	ns/V

1) V_{OE} from 10% V_L to 90%V_L
2) V_{IOVL} from 10%V_L to 90%V_L; V_{IOVCC} from 10%V_{CC} to 90%V_{CC}

Table 6: DC Specification

Symbol	Parameter	Test Condition			Value					Unit
		$V_{L(*)}$ (V)	$V_{CC(*)}$ (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ	Max.	Min.	Max.	
V_{IHL}	High Level Input Voltage (I/O_{VL})	1.8	V_L to 5.5		V_L-0.2			V_L-0.2		V
		2.5	V_L to 5.5		0.75V_L			0.75V_L		
		3.3	V_L to 5.5		0.75V_L			0.75V_L		
		5.0	V_L to 5.5		0.75V_L			0.75V_L		
V_{ILL}	Low Level Input Voltage (I/O_{VL})	1.8	V_L to 5.5				0.15		0.15	V
		2.5	V_L to 5.5				0.30		0.30	
		3.3	V_L to 5.5				0.30		0.30	
		5.0	V_L to 5.5				0.30		0.30	
V_{IHC}	High Level Input Voltage (I/O_{VCC})	1.8	V_L to 5.5		V_L-0.2			V_L-0.2		V
		2.5	V_L to 5.5		0.75V_{CC}			0.75V_{CC}		
		3.3	V_L to 5.5		0.75V_{CC}			0.75V_{CC}		
		5.0	V_L to 5.5		0.75V_{CC}			0.75V_{CC}		
V_{ILC}	Low Level Input Voltage (I/O_{VCC})	1.8	V_L to 5.5				0.15		0.15	V
		2.5	V_L to 5.5				0.30		0.30	
		3.3	V_L to 5.5				0.30		0.30	
		5.0	V_L to 5.5				0.30		0.30	
V_{IH-TS}	High Level Input Voltage (OE)	1.8	V_L to 5.5		V_L-0.2			V_L-0.2		V
		2.5	V_L to 5.5		0.75V_L			0.75V_L		
		3.3	V_L to 5.5		0.75V_L			0.75V_L		
		5.0	V_L to 5.5		0.75V_L			0.75V_L		
V_{IL-TS}	Low Level Input Voltage (OE)	1.8	V_L to 5.5				0.15		0.15	V
		2.5	V_L to 5.5				0.25V_L		0.25V_L	
		3.3	V_L to 5.5				0.25V_L		0.25V_L	
		5.0	V_L to 5.5				0.25V_L		0.25V_L	
V_{OHL}	High Level Output Voltage I/O_{VL}	1.8 to 5.5	V_L to 5.5	I_O=-20 µA $I/O_{VCC} \geq V_{CC}$-0.2	0.67V_L			0.67V_L		V
V_{OLL}	Low Level Output Voltage I/O_{VL}			I_O=1.0 mA $I/O_{VCC} \leq$0.15V			0.40		0.40	
V_{OHC}	High Level Output Voltage I/O_{VCC}	1.8 to 5.5	V_L to 5.5	I_O=-20 µA $I/O_{VL} \geq V_L$-0.2	0.67V_{CC}			0.67V_{CC}		V
V_{OLC}	Low Level Output Voltage I/O_{VCC}			I_O=1.0 mA $I/O_{VL} \leq$0.15V			0.40		0.40	
I_{TSL}	Control Input Leakage Current (OE)	1.8 to 5.5	V_L to 5.5	V_I=GNDor5.5			1		1	µA
I_{TS-LKG}	High Impedance Input Leakage Current (IO_{VL}, I/O_{VCC})	1.8 to 5.5	V_L to 5.5	OE = GND			1		1	µA
I_{QVCC}	Quiescent Supply Current V_{CC}	1.8 to 5.5	V_L to 5.5	I/O_{VL}, I/O_{VCC} unconnected		0.1	1		10	µA
I_{QVL}	Quiescent Supply Current V_L	1.8 to 5.5	V_L to 5.5	I/O_{VL}, I/O_{VCC} unconnected		13	20		100	µA

Symbol	Parameter	Test Condition			Value					Unit
		$V_{L(*)}$ (V)	$V_{CC(*)}$ (V)		T_A = 25 °C			-40 to 85 °C		
					Min.	Typ	Max.	Min.	Max.	
I_{TS-VCC}	High Impedance Mode Quiescent Supply Current V_{CC}	1.8 to 5.5	V_L to 5.5	OE= GND			1		1	µA
I_{TS-VL}	High Impedance Mode Quiescent Supply Current V_L	1.8 to 5.5	V_L to 5.5	OE= GND I/O_{VL} = GND or V_L I/O_{VCC} = GND or V_{CC}			1		1	µA

1) Typical values are referred to T_A=25°C
2) Power Supply Range: V_L, V_{CC} 1.8V±5%, 2.5±0.2V, 3.3±0.3V, 5.0±0.5V
5) For normal operation, ensure $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ will not damage the device

Table 7: AC Electrical Characteristics

Symbol	Parameter		Test Condition(5)		Value			Unit
			C_L=15pF t_r=t_f ≤ 6ns Driver output R_T ≤ 50Ω (8)		-40 to +85 °C			
			V_L (V)(2)	V_{CC} (V)(2)	Min.	Typ.(1)	Max.	
t_{RVCC}	Rise Time I/O_{VCC}(3)(8)		1.8	1.8		11	15	ns
			1.8	5.0		9	15	
t_{FVCC}	Fall Time I/O_{VCC}(3)		1.8	1.8		6	15	ns
			1.8	5.0		10	15	
t_{RVL}	Rise Time I/O_{VL}(3)		1.8	1.8		12	15	ns
			1.8	5.0		10	15	
t_{FVL}	Fall Time I/O_{VL}(3)		1.8	1.8		7	15	ns
			1.8	5.0		7	15	
$t_{IOVL-VCC}$	Propagation Delay Time(4) I/O_{VL-LH} to I/OV_{CC-LH} I/O_{VL-HL} to I/OV_{CC-HL}	t_{PLH}	1.8	1.8		6	15	ns
			1.8	5.0		7	15	
		t_{PHL}	1.8	1.8		5	15	
			1.8	5.0		8	15	
$t_{IOVCC-VL}$	Propagation Delay Time(4) I/OV_{CC-LH} to I/O_{VL-LH} I/OV_{CC-HL} to I/O_{VL-HL}	t_{PLH}	1.8	1.8		2	15	ns
			1.8	5.0		2	15	
		t_{PHL}	1.8	1.8		5	15	
			1.8	5.0		6	15	
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output Enable and Disable Time		1.8	1.8		38	60	ns
			1.8	5.0		44	60	
D_R	Maximum Data Rate		1.8	1.8	13			Mbps
			1.8	5.0	13			
t_{OSLH} t_{OSHL}	Channel to Channel Skew Time (note 6, 7)		1.8	1.8		0.1	1	ns
			1.8	5.0		0.5	1	ns

1) Typical values are referred to T_A=25°C
2) Power Supply Range: V_L, V_{CC} 1.8V±5%, 2.5±0.2V, 3.3±0.3V, 5.0±0.5V.
3) Rise Time:10% to 90%, Fall Time 90% to 10%
4) tpd: 50% to 50%
5) For normal operation, ensure $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ will not damage the device
6) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$
7) Each translator equally loaded; parameter guaranteed by design
8) For $V_{CC} = V_L = 1.8V$, $t_r = t_f \leq 4ns$

Table 8: AC Electrical Characteristics

Symbol	Parameter		Test Condition(5)		Value			Unit
			C_L=15pF t_r=t_f ≤ 6ns Driver output R_T ≤ 50Ω		-40 to +85 °C			
			V_L (V)(2)	V_{CC} (V)(2)	Min.	Typ.(1)	Max.	
t_{RVCC}	Rise Time I/O_{VCC}(3)		1.8	2.5		11	15	ns
			1.8	3.3		10	15	
			2.5	3.3		8	15	
t_{FVCC}	Fall Time I/O_{VCC}(3)		1.8	2.5		7	15	ns
			1.8	3.3		8	15	
			2.5	3.3		6	15	
t_{RVL}	Rise Time I/O_{VL}(3)		1.8	2.5		10	15	ns
			1.8	3.3		9	15	
			2.5	3.3		7	15	
t_{FVL}	Fall Time I/O_{VL}(3)		1.8	2.5		6	15	ns
			1.8	3.3		6	15	
			2.5	3.3		4	15	
$t_{IOVL-VCC}$	Propagation Delay Time(4) I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	1.8	2.5		7	15	ns
			1.8	3.3		7	15	
			2.5	3.3		4	15	
		t_{PHL}	1.8	2.5		5	15	
			1.8	3.3		6	15	
			2.5	3.3		4	15	
$t_{IOVCC-VL}$	Propagation Delay Time(4) I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	1.8	2.5		2	15	ns
			1.8	3.3		2	15	
			2.5	3.3		2	15	
		t_{PHL}	1.8	2.5		5	15	
			1.8	3.3		5	15	
			2.5	3.3		4	15	
t_{PZL} t_{PZH} t_{PLZ} t_{PHZ}	Output Enable and Disable Time		1.8	2.5		38	60	ns
			1.8	3.3		38	60	
			2.5	3.3		23	40	
D_R	Maximum Data Rate		1.8	2.5	13			Mbps
			1.8	3.3	13			
			2.5	3.3	13			

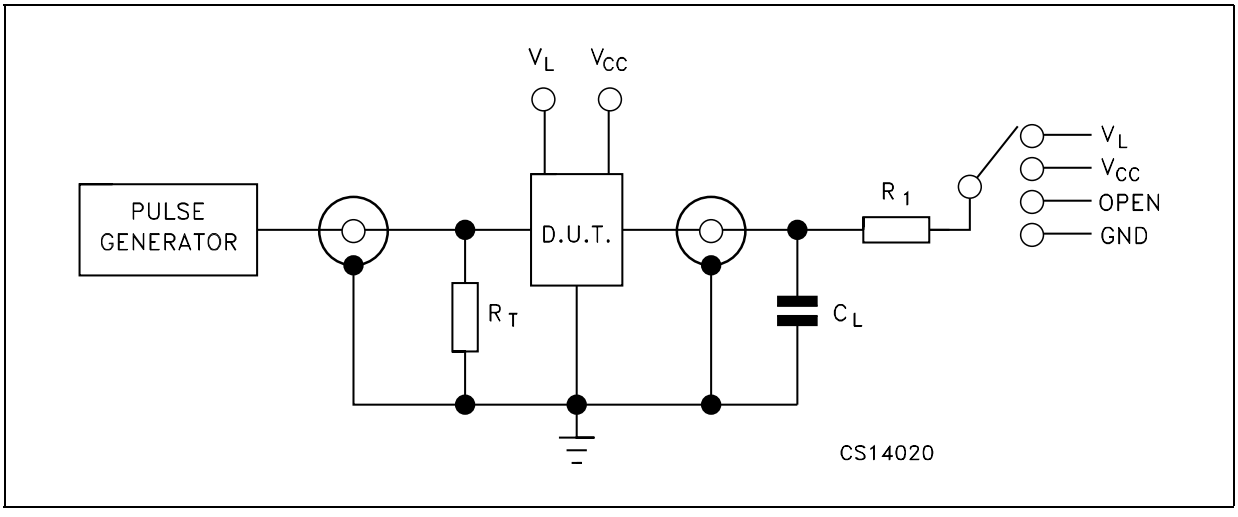
1) Typical values are referred to T_A=25°C
2) Power Supply Range: V_L, V_{CC} 1.8V±5%, 2.5±0.2V, 3.3±0.3V, 5.0±0.5V.
3) Rise Time:10% to 90%, Fall Time 90% to 10%
4) tpd: 50% to 50%
5) For normal operation, ensure V_L< (V_{CC} + 0.3V). During power-up, V_L > (V_{CC} + 0.3V) will not damage the device
6) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW (t_{OSLH} = | t_{PLHm} - t_{PLHn}|, t_{OSHL} = | t_{PHLm} - t_{PHLn}|
7) Each translator equally loaded; parameter guaranteed by design

Table 9: AC Electrical Characteristics - Open-drain Driving

Symbol	Parameter		Test Condition(5)		Value			Unit
			C_L=15pF Driver output $R_T \leq 50\Omega$		-40 to +85 °C			
			V_L (V)(2)	V_{CC} (V)(2)	Min.	Typ.(1)	Max.	
t_{RVCC}	Rise Time I/O_{VCC}(3)		1.8	1.8		210	300	ns
			1.8	5.0		59	150	
t_{FVCC}	Fall Time I/O_{VCC}(3)		1.8	1.8		12	30	ns
			1.8	5.0		20	30	
t_{RVL}	Rise Time I/O_{VL}(3)		1.8	1.8		210	300	ns
			1.8	5.0		96	150	
t_{FVL}	Fall Time I/O_{VL}(3)		1.8	1.8		11	30	ns
			1.8	5.0		11	30	
$t_{IOVL-VCC}$	Propagation Delay Time(4) I/O_{VL-LH} to I/O_{VCC-LH} I/O_{VL-HL} to I/O_{VCC-HL}	t_{PLH}	1.8	1.8		210	300	ns
			1.8	5.0		100	150	
		t_{PHL}	1.8	1.8		7	20	
			1.8	5.0		14	20	
$t_{IOVCC-VL}$	Propagation Delay Time(4) I/O_{VCC-LH} to I/O_{VL-LH} I/O_{VCC-HL} to I/O_{VL-HL}	t_{PLH}	1.8	1.8		210	300	ns
			1.8	5.0		57	150	
		t_{PHL}	1.8	1.8		7	20	
			1.8	5.0		8	20	
D_R	Maximum Data Rate		1.8	1.8	800			Kbps
			1.8	5.0	800			
t_{OSLH} t_{OSHL}	Channel to Channel Skew Time (note 6, 7)		1.8	1.8		10	20	ns
			1.8	5.0		2	10	ns

1) Typical values are referred to T_A=25°C
2) Power Supply Range: V_L, V_{CC} 1.8V±5%, 2.5±0.2V, 3.3±0.3V, 5.0±0.5V.
3) Rise Time:10% to 90%, Fall Time 90% to 10%
4) tpd: 50% to 50%
5) For normal operation, ensure $V_L < (V_{CC} + 0.3V)$. During power-up, $V_L > (V_{CC} + 0.3V)$ will not damage the device
6) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = | t_{PLHm} - t_{PLHn} |$, $t_{OSHL} = | t_{PHLm} - t_{PHLn} |$
7) Each translator equally loaded; parameter guaranteed by design

Figure 3: Test Circuit



TEST	Switch		
	Driving I/O_{VL}	Driving I/O_{VCC}	Open Drain Driving
t_{PLH}, t_{PHL}	Open	Open	Open
t_{PZL}, t_{PLZ}	V_{CC}	V_L	-
t_{PZH}, t_{PHZ}	Gnd	Gnd	-

C_L = 15/50pF or equivalent (includes jig and probe capacitance)
R1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

Table 10: Waveform Symbol Value

Symbol	Driving I/O_{VL}		Driving I/O_{VCC}	
	$1.8V \le V_L \le V_{CC} \le 2.5V$	$3.3V \le V_L \le V_{CC} \le 5.0V$	$1.8V \le V_L \le V_{CC} \le 2.5V$	$3.3V \le V_L \le V_{CC} \le 5.0V$
V_{IH}	V_L	V_L	V_{CC}	V_{CC}
V_{IM}	50% V_L	50% V_L	50% V_{CC}	50% V_{CC}
V_{OM}	50% V_{CC}	50% V_{CC}	50% V_{CC}	50% V_{CC}
V_X	V_{OL} +0.15V	V_{OL} +0.3V	V_{OL} +0.15V	V_{OL} +0.3V
V_Y	V_{OH} -0.15V	V_{OH} -0.3V	V_{OH} -0.15V	V_{OH} -0.3V

Figure 4: Waveform - Propagation Delay (f=1MHz; 50% duty cycle)

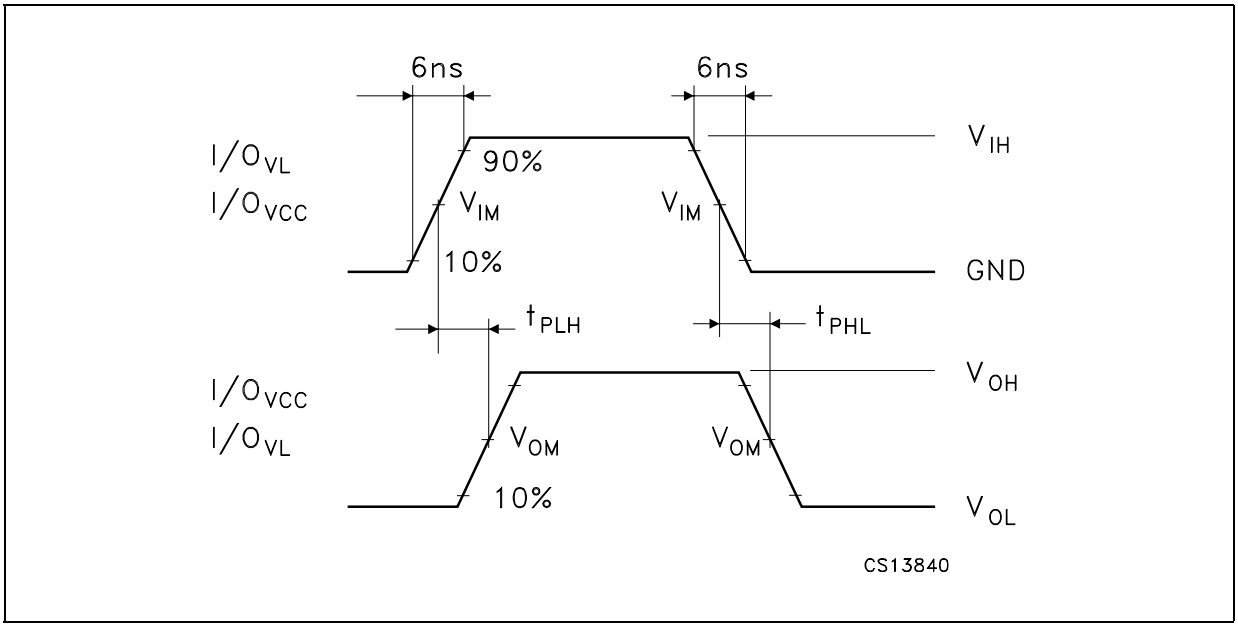
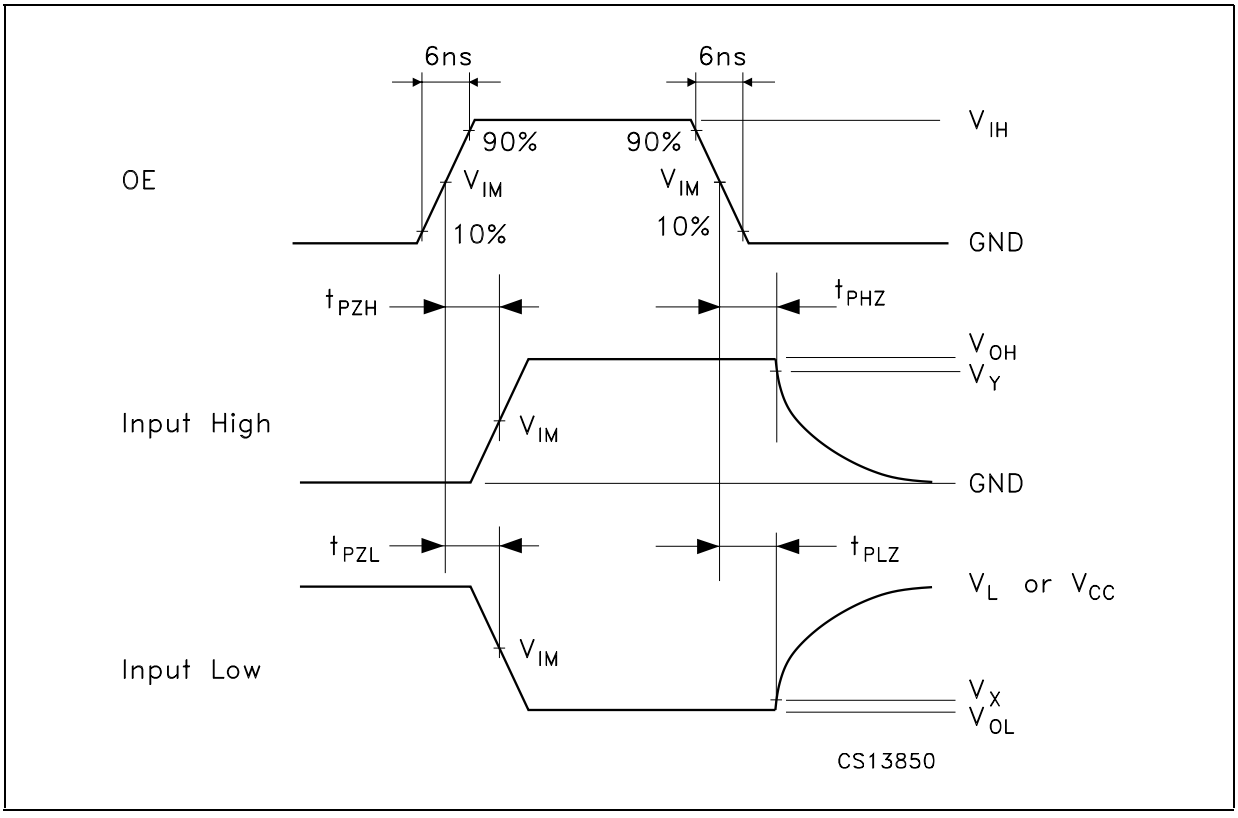
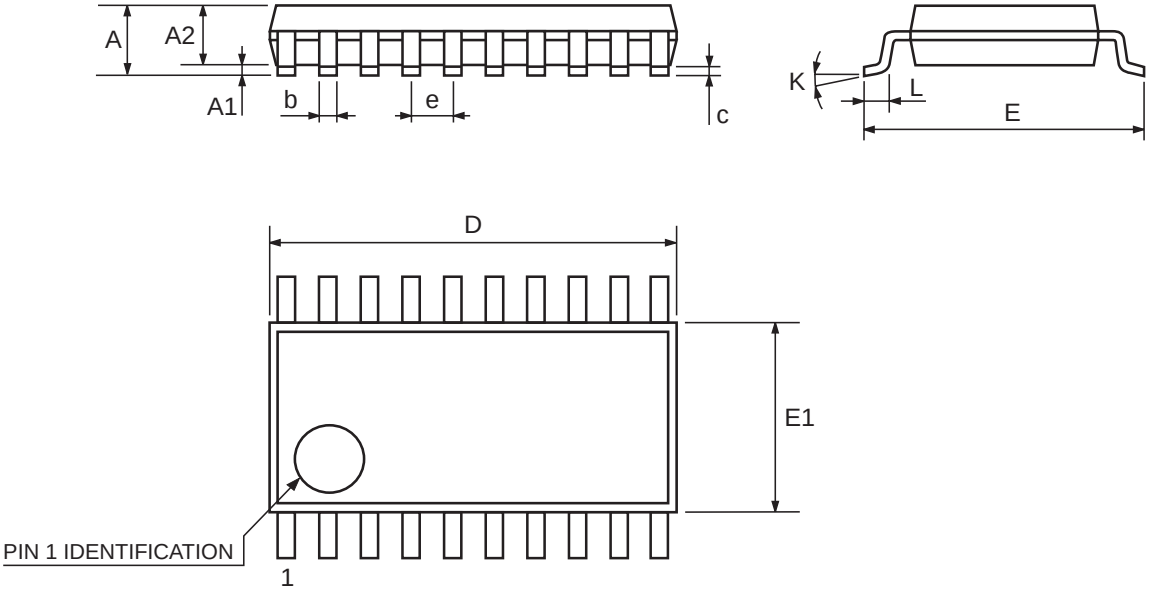


Figure 5: Waveform - Output Enable And Disable Time (f=1MHz; 50% duty cycle)



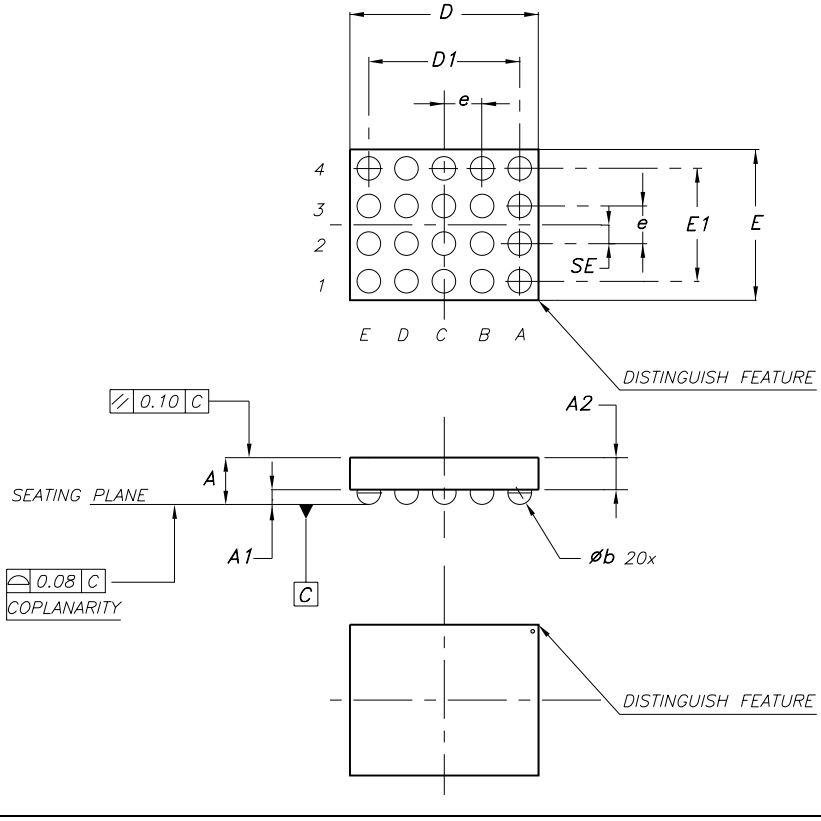
TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0079
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



Flip-Chip20 MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.81	0.89	1.00	31.9	35.0	39.4
A1	0.15	0.24	0.35	5.9	9.4	13.8
A2		0.65			25.6	
b	0.25	0.30	0.35	9.8	11.8	13.8
D	2.41	2.46	2.51	94.9	96.9	98.8
D1		2.00			78.7	
E	1.93	1.98	2.03	76.0	78.0	79.9
E1		1.5			59.1	
e		0.50			19.7	
SE		0.25			9.8	



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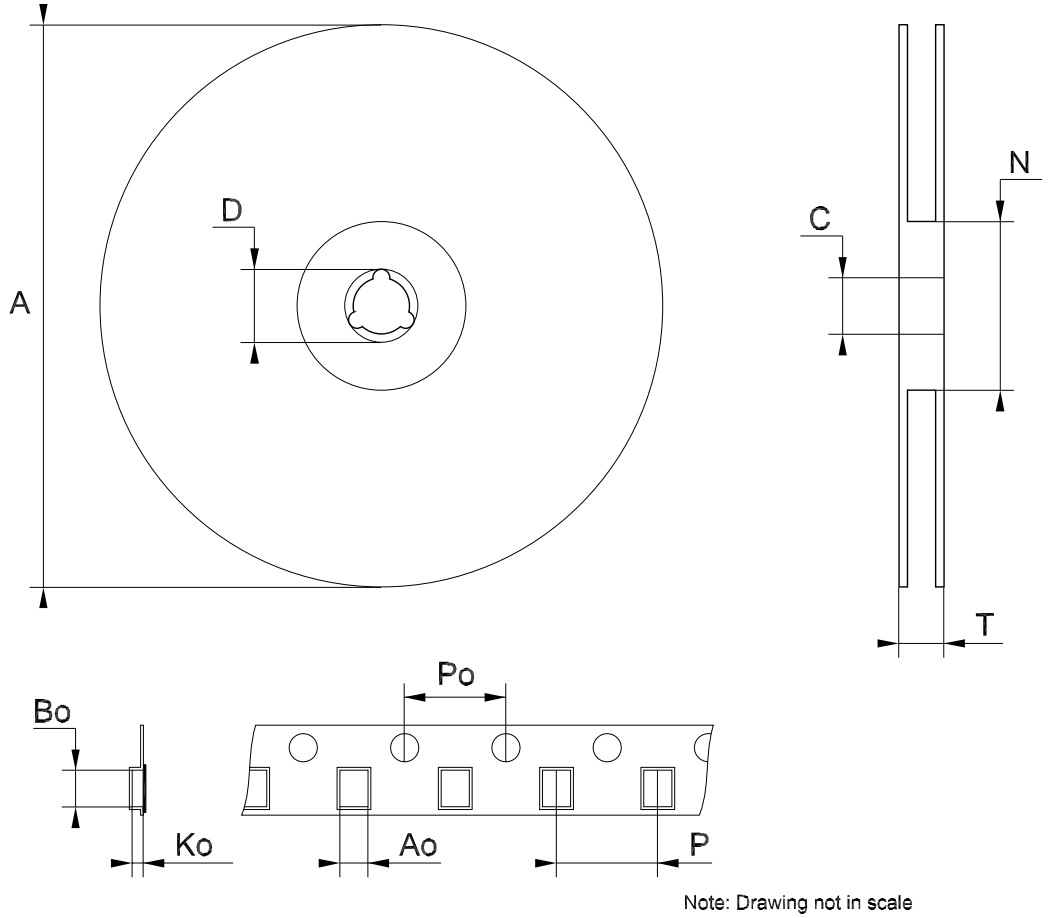
Tape & Reel Flip-Chip20 MECHANICAL DATA

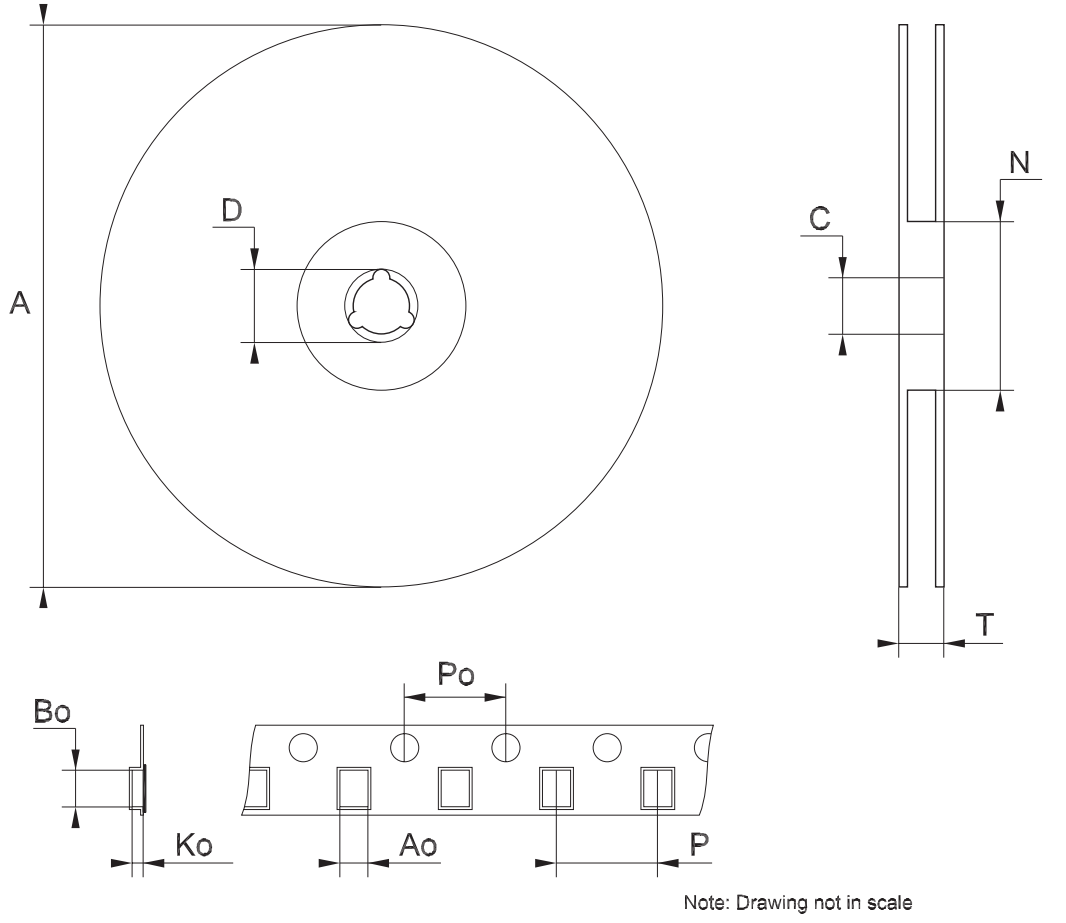
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	2.13	2.23	2.33	0.084	0.088	0.092
Bo	2.62	2.72	2.82	0.103	0.107	0.111
Ko	1.05	1.15	1.25	0.041	0.045	0.049
Po	3.9		4.1	0.153		0.161
P	3.9		4.1	0.153		0.161



Note: Drawing not in scale

Tape & Reel TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	6.9		7.1	0.272		0.280
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

Table 11: Revision History

Date	Revision	Description of Changes
11-Mar-2005	5	Flip-Chip20 Mechanical Data: New Release.